REMARKS

Claims 1-16 and 18 are pending in the application.

Claim 16 has been amended in order to more particularly point out and distinctly claim the subject matter to which the applicant regards as his invention.

Claim Rejections under 35 USC §112

Claim 17 is rejected under 35 USC §112, second paragraph, as being indefinite, for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 17 has been canceled, thus rendering the above rejection moot. Therefore, withdrawal of the rejection of Claim 17 under 35 USC §112, second paragraph, is respectfully requested.

Claim Rejections under 35 USC §103

Claims 16-18 are rejected under 35 USC §103(a) as being unpatentable over admitted Prior Art Figure 8 and Gwen et al. (U.S. Patent No. 5,472,892).

Figure 8 describes an integrated circuit in the prior art having a flash memory (A), a low voltage transistor (B), and mid-level voltage transistor (D), and a high voltage transistor (C). A semiconductor substrate is used as the base for each of the foregoing devices. In addition, insulation (12B) is shown with a thickness of 1.5-5 nm, insulation (12D) is shown with a thickness of 5-10 nm, and insulation (12C) has a thickness of 8-50 nm. In addition, gate electrode (16), as solely illustrated by figure 8J, appears to illustrate electrodes 16 of equal height. A floating gate (13) with a control gate (16) is formed on the silicon gate (13) using an ONO film (14), as shown in figure 8B.

Gwen et al. describes the method of the manufacturing gate memory in which a silicon layer (206) is placed in a cell array region and a silicon layer (208) is placed in a peripheral circuit region. According to figure 3I, silicon layer (208) appears to be placed directly upon silicon layer (206).

The Admitted Prior Art merely shows the first through third MOS transistors having respective gate electrodes, wherein it should be noted that each of the gate electrodes is formed of a single polysilicon layer.

Gwen et al. is also silent about the feature of the first gate electrode being formed of lamination of the first silicon film and the second silicon film and the second gate electrode formed of lamination of the third silicon film and the second silicon film. In Fig. 3I of Gwen, it is also noted that there is interposed an interlayer insulation film 205 between the polysilicon layer 204 and the polysilicon layer 206. This means that there is formed a flash memory cell, not a MOS transistor in Fig. 3I of Gwen. In order to use this flash memory cell structure of the gate electrode of a MOS transistor, Gwen connects the polysilicon layer 204 with the polysilicon layer 208 via a contact hole as represented in Fig. 3J.

The prior art relied upon by the Examiner does not disclose or suggest a second gate electrode having a second silicon film stacked upon a third silicon film. Specifically, independent claims 16 patentably distinguishes over the prior art relied upon, by reciting,

> "A semiconductor integrated circuit, comprising: a semiconductor substrate; a non-volatile memory formed in a memory cell region of said semiconductor substrate; a first MOS transistor formed on a first device region of said semiconductor substrate, said first MOS transistor having a first gate insulation film of first thickness and a first gate electrode; a second MOS transistor formed on a second device region of said semiconductor substrate, said second MOS transistor having a second gate oxide film of second thickness and a second gate electrode; and

a third MOS transistor formed on a third device region of said semiconductor substrate, said third MOS transistor having a third gate insulation film of third thickness and a third gate electrode; said first thickness being smaller than said second thickness, said second thickness being smaller than said third thickness, said first through third gate electrodes having a substantially identical height, wherein said first and third gate electrodes have a structure in which a second silicon film is stacked on a first silicon film, said second gate electrode has a structure in which said second silicon film is stacked on a third silicon film, and wherein said non-volatile memory is formed of a floating gate electrode formed of said third silicon film and a control gate electrode formed on said floating gate electrode via an insulation film and having a structure in which said first silicon film and said second silicon film are consecutively stacked." (Emphasis Added)

Therefore, withdrawal of the rejection of Claims 16-18 under 35 USC §103(a) as being unpatentable over admitted Prior Art Figure 8 and Gwen et al. (U.S. Patent No. 5,472,892) is respectively requested.

Conclusion

The above amendments are believed to place the claims in proper condition for examination. Early and favorable action is awaited.

Attached hereto is a marked-up version of the changes made to the claim by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In the event that any fees are due in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

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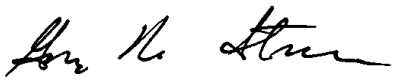

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VERSION WITH MARKINGS TO SHOW CHANGES MADE (09/960,399)

IN THE CLAIMS:

Amend claim 16 as indicated below:

16. (Amended) A semiconductor integrated circuit, comprising:

a semiconductor substrate;

a non-volatile memory formed in a memory cell region of said semiconductor substrate;

a first MOS transistor formed on a first device region of said semiconductor substrate, said first MOS transistor having a first gate insulation film of first thickness and a first gate electrode;

a second MOS transistor formed on a second device region of said semiconductor substrate, said second MOS transistor having a second gate oxide film of second thickness and a second gate electrode; and

a third MOS transistor formed on a third device region of said semiconductor substrate, said third MOS transistor having a third gate insulation film of third thickness and a third gate electrode;

said first thickness being smaller than said second thickness, said second thickness being smaller than said third thickness,

said first through third gate electrodes having a substantially identical height, [wherein the first, second, and third gate electrode each comprise two silicon layers stacked one upon the other] wherein said first and third gate electrodes have a structure in which a second silicon film is stacked on a first silicon film, said second gate electrode has a structure in which said second silicon film is stacked on a third silicon film, and wherein said non-volatile memory is formed of a floating gate electrode formed of said third silicon film and a control gate electrode formed on said floating gate

electrode via an insulation film and having a structure in which said first silicon film and said second silicon film are consecutively stacked.